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DYNAMICALLY PROGRAMMABLE ANALOG ARRAYS IN ACOUSTIC FREQUENCY RANGE SIGNAL PROCESSING

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Abstract

Field programmable analog arrays (FPAA), thanks to their flexibility and reconfigurability, give the designers quite new possibilities in analog circuit design. The number of both academic projects on FPAA and applications of commercially available programmable devices is still growing. This paper explores the properties and parameters of two most popular FPAA circuits: the AnadigmVortex AN221E04 and AnadigmApex AN231E04 from the Anadigm company. The research conducted by the authors led to the discovery of some undocumented features of these devices. Several applications for audio processing were built and tested. The results show that these circuits can be used in medium-demanding audio applications. Thanks to dynamic reconfigurability, they also allow to build an universal analog audio signal processor. These circuits can also act as a versatile platform for rapid prototyping and educational purposes.

Keywords: FPAA, audio processing, switched-capacitor, analog circuits design

1. Introduction

Field Programmable Analog Arrays (FPAA) draw rising attention because of their flexibility. They offer a possibility to simplify the design process and to speed up the prototyping of analog circuits. FPAAs also promise a way to miniaturize analog interfaces (especially in measurement systems) because of their ability to be reconfigured in a working circuit.

There are various reported FPAA architectures. Such devices can be built as continuous-time (e.g. OTA-C) and discrete-time (e.g. Switched-Capacitor SC) devices. Both approaches can be found in literature. The next section of this paper will give a short overview of reported FPAAs – their architectures and properties.

Further sections will focus respectively on a brief overview of FPAA applications, parameters of examined devices, their functionality and possible applications in audio signal processing. Work reported in this article confirms that several different analog devices can be designed using the same hardware platform.

2. Overview of FPAA architectures

The FPAAs reported in literature and commercially available can be divided into two groups. One of them is the continuous-time FPAAs group. These devices utilize operational transconductance amplifiers (OTA), analog multipliers or other types of amplifiers with configurable networks of passive components. The second group contains the discrete time devices, mostly based on the switched capacitor (SC) principle. Contrary to digital programmable circuits (eg. FPGA or CPLD), which are commonly available and used, the analog programmable circuits are considered a new branch. There are few vendors that

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deliver commercially available FPAA circuits, while the number of academic projects on programmable analog circuits is still growing.

2.1. Academic projects

The majority of devices encountered in literature are academic projects. According to the authors' knowledge, none of the devices described in this section is available on the market.

2.1.1. Reconfigurable Analog Signal Processor (RASP)

The RASP is an FPAA designed by Tyson S. Hall in his Ph.D. thesis [1]. Since then it has been developed by the CADSP group at Georgia Institute of Technology. The current version is marked 2.8 [2].

It is a large-scale device consisting of 32 Configurable Analog Blocks (CABs) of two types – CAB 1 and CAB 2. CAB 1 employs 3 Operational Transconductance Amplifiers (OTAs) with programmable bias current sources, 3 floating capacitors, 2 multi-input floating-gate transistors (FGFET), a transmission gate and an nMOS/pMOS transistor array. CAB 2 is built of an FGFET-based current mirror, an OTA and 2 folded Gilbert multipliers.

The authors of [2] report that RASP is able to perform AM reception and speech processing. One of the previous generations of this FPAA was reported to be capable of modeling a perceptual model of an MP3 encoder [3].

2.1.2 FPAA by Pankiewicz et al.

Bogdan Pankiewicz *et al.* report an FPAA designed for filtering applications [4]. It was developed as a result of the main author's Ph. D. thesis.

The device comprises 40 CABs built of one OTA and one programmable capacitor each. The CABs are placed in an array of 5 rows and 8 columns with interconnections between neighbouring CABs.

The authors report the design of a sixth-order Chebyshev bandpass filter with center frequency of 60 kHz, tunable in a range of about 22 times. Reported maximum operating frequency of a single CAB in this FPAA is 9 MHz.

2.1.3 FPAA by Univ. of Freiburg and Univ. of Ulm researchers

A team of researchers from University of Ulm and University of Freiburg presented an FPAA of different architecture [5]. It is also built as a continuous-time device (on OTAs and capacitances). Its authors introduce a hexagonal lattice CAB layout, which employs 6 interconnections to neighboring blocks and one for self feedback. Tuning is realized using FGFET switches and current sources.

The latest report on this work [6] states that the designed circuit contains 55 CABs and its Gain-Bandwidth Product (GBP) is 186 MHz.

2.2. Commercially available devices

There are several families of programmable analog circuits commercially available. They differ from one another in principle of operation, amount of resources and area of application.

2.2.1. PSoC family from Cypress Semiconductor [7]

PSoC® is a **programmable embedded system-on-chip** integrating configurable analog and digital peripheral functions, memory and a microcontroller on a single chip. The PSoC® architecture consists of configurable analog and digital blocks, a CPU subsystem and programmable routing and interconnect. PSoC allows to insert a predefined and tested analog and digital circuitry IP from the PSoC library into a project.

The analog system is composed of 12 configurable blocks, each containing an opamp circuit, which allows to create complex analog signal flows. Analog blocks are provided in columns of three, each including one Continuous Time (CT) and two Switched Capacitor (SC) blocks. Analog peripherals are very flexible and can be customized to support specific application requirements.

Some more common PSoC analog functions (mostly available as user modules) are: ADCs (selectable as incremental, delta sigma, and SAR), DACs (with 6- to 9-bit resolution), filters (2-, 4-, 6-, and 8-pole band pass, low pass, and notch), amplifiers (up to 4, with selectable gain to 48x), instrumentation amplifiers (up to 2, with selectable gain to 93x), comparators (up to 4, with 16 selectable thresholds), multiplying DACs (up to 4, with 6- to 9-bit resolution), high current output drivers (four with 30 mA drive as a core resource), 1.3 V reference, DTMF dialer, modulators, correlators, peak detectors and many other topologies.

Each of the analog blocks has to be parameterized and switched on by the CPU software. The program can be written in C or assembler languages. It is also possible to change parameters of particular blocks during runtime.

2.2.2. FPAA and dpASP family from Anadigm [8]

Anadigm offers a full range of 5 V and 3.3 V programmable analog arrays. They are divided into static programmable devices (FPAA), which require a reset before loading a new configuration bitstream, and so called dynamically programmable Analog Signal Processors (dpASP). Anadigm's dpASPs provide real time dynamic reconfigurability that allows the functionality of the dpASPs to be reconfigured in-system by the designer or "on-the-fly" by a microcontroller/processor. A dpASP can be programmed to implement multiple analog functions and/or adapt "on-the-fly" to maintain precision operation required by applications that have changing requirements in real time, such as signal conditioning, filtering, data acquisition, and closed-loop control.

By using AnadigmDesigner2 EDA software, the designer can construct complex analog functions using configurable analog modules (CAMs) as building blocks. With an easy-to-use drag-and-drop interface, the design process can be measured in minutes allowing complete analog systems to be built, immediately simulated, and then downloaded to the dpASP chip for testing and validation.

Programmable analog arrays from the Anadigm company are the most popular commercially available FPAA circuits. This paper is intended to discuss some features of these devices.

2.2.3. ispPAC family from Lattice Semiconductor [9]

The ispPAC family consists of 5 circuits. All of them work according to the continuous time principle and can be programmed in-system. The circuits have different functionality. They can work as variable gain amplifiers, instrumental amplifiers, analog signal adders, subtractors, integrators, programmable filters etc. All the ispPAC circuits can be programmed using Lattice's PAC-Designer design tools. Circuit designs are entered graphically and

verified all within a single environment. The PAC-Designer schematic window provides access to all programmable features in ispPAC devices via a graphical user interface. Once the design file is complete, it can be saved and an industry-standard JEDEC file can be generated for device programming. The ispPAC circuits are intended for a wide variety of analog signal conditioning.

In 2007 the production of ispPAC circuits was discontinued and there are no replacement parts for them [10].

2.2.4. Other devices

There are several more FPAA families the production of which is discontinued. An example is the TRAC family from Zetex Semiconductors [11]. The circuits contained 20 simple configurable analog blocks working in continuous time. Another example is the MPAA020 from Motorola [12]. It also contained 20 cells working on the SC principle. This circuit is not produced now but the idea was continued by the Anadigm Company in the AN10E40 device. Modern successors of these solutions are the dpASP circuits discussed in this paper.

3. FPAA applications in literature

Numerous FPAA applications reported in literature are based on dpASP circuits from Anadigm. These circuits are implemented in acoustic signal processing, medical signal processing and also in measurement instruments. Some of them utilize dynamic reconfiguration of the circuit. As an example we can mention an ultrasonic proximity meter in which the filter parameters are changing adaptively, which improves the measurement accuracy [13]. Another example of FPAA application is an adaptive conditioning circuit in which the resolution enhancement was obtained using dynamic reconfigurability of AN231E04 [14]. FPAAs are also used as analog computers, for example for modeling of power system dynamics. Comparing with numerical analysis, FPAA modeling significantly shortened the simulation time, providing acceptable accuracy [15]. There are also applications of PID controllers based on FPAA. Thanks to dynamic reconfiguration it is possible to build a self-tuning PID controller in which the signal path is fully analog [16].

Also some medical applications can be found like a smart stethoscope based on FPAA [17] or adaptive circuit that detects QRS complexes in an ECG signal [18].

4. The scope of this work

This work focuses on Anadigm devices. It results from their versatility and ability to be reconfigured “on-the-fly”, during the operation of the circuit. However, not every parameter of these devices is properly specified, so it has been decided to examine parameters of Anadigm FPAAs in our Institute. Particular effort has been put into examining reconfiguration capability, distortion and noise parameters, and antialiasing filter behavior. We have also developed some simple audio processing circuits to verify the measurements and determine a possible scope of applications of the FPAAs.

5. An overview of examined devices

Anadigm offers two families of FPAA. One of them is AnadigmVortex, powered from a 5 V supply. The AnadigmApex family is a successor of AnadigmVortex. One of the most noticeable differences between them is the supply voltage - the new Apex family is powered

from a 3.3 V supply instead of the 5 V one. This results in easy interfacing to contemporary 3.3 V microcontrollers with no need of using level-shifters. The power consumption has not changed significantly. Both AN231 and AN221 with comparable configurations and a 16 MHz clock require about 45 mA of current [19], [20].

Both families include 2x2 Configurable Analog Blocks (CAB) array. Each CAB consists of 2 operational amplifiers, 8 programmable capacitors, a Successive-Approximation register and a comparator. All analog signal paths are fully differential. Chip architecture includes also a Lookup Table (LUT) for realizing nonlinear transfer functions.

The configuration RAM of the chip is divided into the configuration memory and shadow memory. When the FPAA is working, it is set up in accordance to the configuration memory. New configuration data received by the SPI interface is stored in the shadow memory. Configuration changes do not take effect until the FPAA receives an "Execute" signal, which can be generated externally or internally (by an event or on configuration data transfer completion).

6. Comparison of Apex and Vortex families

6.1 IO Cells

The main functional difference between Apex and Vortex families is the number and structure of IO cells. The Vortex family contains 4 input cells with an output option, 2 dedicated output cells and 1 auxiliary output cell. Each of the input cells can work with gain in the range from 16 to 128 or in the bypass mode. In addition, when a cell is programmed in the gain mode, the chopper amplifier can be enabled to nullify the input offset voltage. Each of the input cells has also a programmable lowpass anti-alias filter with corner frequency ranging from 76 to 470 kHz. One of the input cells is connected to an input multiplexer providing a possibility to select one of four input differential channels or eight single ended channels.

Output cells of the Vortex-family FPAA can be configured as either analog or digital. Analog output cells have smoothing lowpass filters with the same frequency range as the input antialiasing filters. An output cell can also work in the bypass mode.

The Apex-family device has 7 IO cells in total and 1 auxiliary 2-output cell. There are 4 Type1 and 3 Type2 cells. Each of the Type1 cells can work as an input or output cell. When configured as an input, a Type1 cell can work in the bypass mode, as a fully-differential amplifier or as a sample-and-hold (S/H) circuit. In addition, two out of four Type1 cells can access a chopper amplifier.

Type1 cell used as an output can work in the bypass mode, as a S/H circuit or as a digital output (for comparator signal output). It can also output a 1.5 V reference voltage (VMR).

Type2 cells can be set as a bypass input, digital input (for controlling internal comparators), bypass output, digital output or VMR output. In the digital output mode a Type2 cell can output a clock signal, a comparator output signal or a RAM-transfer pulse indicating a configuration change. In the input mode one of the Type2 cells can access a chopper amplifier.

AN231 FPAA includes a single chopper amplifier with programmable gain feature accessible from one selected IO cell. The gain ranges from 0 to 60 dB. Besides that, OpAmp chopping can be enabled for each of the gain-stage CAMs in the FPAA.

AN231's IO cells do not include anti-aliasing filters. It is up to the user to design an anti-aliasing and smoothing filter using a differential amplifier of a Type1 cell and external resistors and capacitors. Anadigm provides the formulas to determine the values of components in the anti-aliasing filters with the required corner frequency.

6.2 Chip clocks

Switched-capacitor (SC) circuits require clock signals. Both examined devices have to be clocked externally. However, none of available CAMs can be clocked with maximum clock frequency. Both examined devices include internal frequency dividers generating non-overlapping clock signals for the FPAA core.

AN221 has 1 main (system-wide) and 4 local frequency dividers with divisors ranging from 1 to 510. The clock frequency is divided in a cascade of the main and one of the local dividers, which enables the circuit to be dynamically tuned by changing only the main clock divisor.

AN231 is equipped with 2 system-wide and 6 local dividers. The clock source of local dividers is selectable by the user. Moreover, two of the local dividers can generate clocks with a tunable phase delay referring to the clock source.

7. Estimation of THD and SFDR

7.1 AN221 (Vortex)

An important parameter characterizing the quality of analog circuit is Total Harmonic Distortion (THD). It can be treated as a measure of nonlinearity of an analog signal path. In order to measure this parameter, a circuit comprising an input cell with an antialiasing filter, an inverting amplifier and an output cell with a smoothing filter has been realized in the AN221E04 matrix.

A surprisingly high level of distortion – about 0.25% – has been measured. It did not change after removing the amplifier, but it depended on the corner frequency of the input or output filter. It was noticed that the lower the corner frequency of the filter, the higher the THD, while theoretically the low pass filtering should decrease the THD. Almost the same level of THD is introduced by the input and output filters.

In order to explain the observed effect the pulse responses were registered for different amplitudes and different corner frequencies of the filters. The responses to two different amplitudes at a corner frequency of 100 kHz are shown in Fig. 1a and 1b.

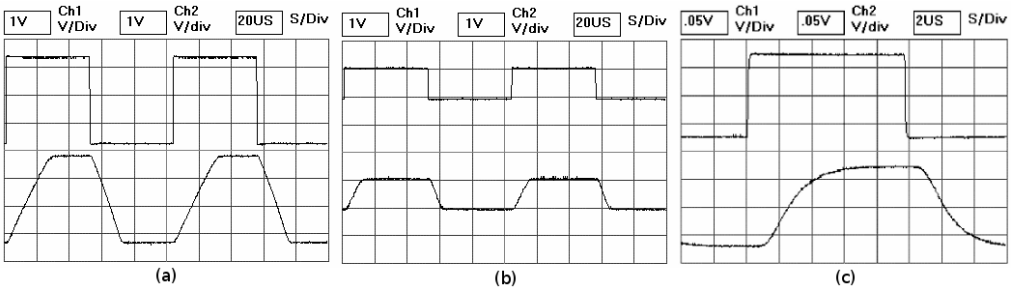

Fig. 1. Pulse response for large (a), small (b) and very small (c) amplitude

One can see that the pulse responses in both cases have the same slew rate, but the rise time is different. This feature is typical for the circuits with slew limitation, i.e. nonlinear circuits. Another drawback of the circuit is different slew rates for the rising edge (about 0.1 V/μs) and falling edge (about 0.15 V/μs). For the input voltages below 0.2 $V_{p\text{-}p}$ the pulse response is typical for linear circuits, i.e. constant rise time and the rate of edges proportional to the amplitude (Fig. 1c).

For the corner frequency of 400 kHz the results were analogous – slew rate 0.8 V/μs for the rising edge, 0.5 V/μs for the falling edge and a constant rise time for the input amplitude below 0.6 V.

It leads to the conclusion that if a low THD level is required, the internal anti-aliasing filters and smoothing filters should be bypassed and replaced by external continuous-time filters. Unfortunately, it causes a growth of costs and increases the PCB area of the application.

7.2 AN231 (Apex)

To estimate the THD in the AN231E04 matrix, several simple device applications were created. Additionally a symmetrizing operational amplifier was added to the input of the FPAA.

Table 1: FPAA configurations and measured THD and SFDR values

Meas. number	Input cell	Output cell	Gain stage	THD level	SFDR level
1	External symmetrizing OpAmp			0.038%	72.60 dB
2	Bypass	Bypass	None	0.103%	60.15 dB
3	Filter	Bypass	None	0.187%	54.85 dB
4	Filter	Filter	None	0.139%	58.43 dB
5	Filter	Filter	Unity gain	0.198%	58.30 dB
6	Filter	Filter	Gain of 5	0.181%	58.04 dB
7	Automatic Gain Control			0.471%	42.95 dB

Table 1 summarizes all tested configurations and gives the values of measured harmonic distortion and Spurious-Free Dynamic Range (SFDR). The first row in the table gives the result of measuring of the output signal of the symmetrizing operational amplifier. The last row gives the result for an Automatic Gain Control circuit. The source generator has a distortion level of 0.006%, SFDR of 84.4 dB and output amplitude of 1 V (except for the measurement of gain-of-5 stage, when a 0.2 V amplitude was set). An exemplary spectrum graph taken during measurements from an HP 35665A spectrum analyzer is presented in Fig. 2. Comparing the obtained results with those described in the previous section it can be noticed that input and output filters in AN231 device introduce less harmonic distortion than in the AN221 FPAA. This is because the AN231 uses differential operational amplifiers as antialiasing and smoothing filter cores. The corner frequency adjustment is made by the user with changes of external component values – Anadigm resigned from antialiasing filters inside the matrix's IO cells.

Measurement results show that the AN231 FPAA introduces a similar level of THD into a processed signal as a digital guitar-effect KORG AX3G. With an input signal amplitude of 0.5 V and a frequency of 2 kHz the AN231 FPAA introduced a THD of 0.118% while the AX3G in bypass mode introduced a THD of 0.135%.

Table 2 shows a listing of distortion parameters measured in this work, the works reported and the datasheets of circuits described in section 2 of this article. The direct comparison of these parameters is, however, not possible due to different measurement conditions in each of the mentioned works. For the Cypress PSoC devices none of the distortion parameters are available.

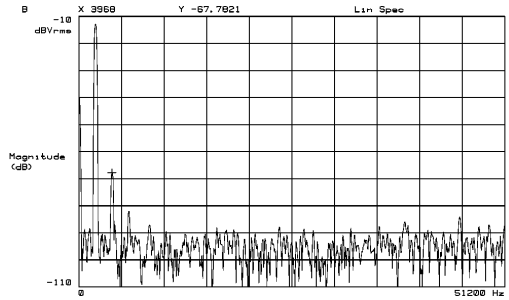

Fig. 2. Spectrum of FPAA output signal — measurement 3 of 7 (Table 1)

Table 2: Listing of the distortion parameters of reported circuits.

Parameter	**this work (IN cell)**	**RASP [2]**	**FPAA by Becker [6]**	**TRAC020 [11]**	**AN231E04 [19]**	**AN221E04 [20]**	**ispPAC 10 [23]**
THD	54.5 dB	n/a	n/a	n/a	n/a	65 dB	74 dB
SFDR	54.85 dB	65.2 dB	50 dB	50 dB	96 dB	73 dB	n/a

7.3 Automatic Gain Control Circuit

An automatic gain control circuit (AGC) is used to change the voltage gain in order to regulate the signal output level at the value possibly close to the preset one. There are also similar circuits that dynamically change the gain according to the input signal level – for example level compressors and level limiters commonly used in acoustic signal processing applications. The idea is always the same but the transfer characteristics differ.

An AGC circuit requires an analog multiplier or other amplifier with the electrically controlled voltage gain factor (Variable Gain Amplifier, VGA), for example a transconductance amplifier. The CAM library of the AN221E04 contains a SC amplifier block called GainVoltageControlled. In this circuit the capacitance values that determine the gain factor are set dynamically depending on the conversion result from the SAR analog-to-digital converter measuring the control voltage signal.

The AGC circuit realized using AN221E04 device works in the acoustic frequency range. The block diagram of the circuit created in an AnadigmDesigner2 environment is shown in Fig. 3a.

The features and parameters of this circuit were studied in detail in [21].

The circuit gave proper output level for the input signal amplitude over a two-decade range, from 40 mVpp up to 4 Vpp. These values correspond to the preset gain range (from 0.3 up to 50) of the voltage controlled amplifier stored in the LUT.

The output level and the response time constant could be tuned using the dynamic reconfigurability feature.

The most curious feature discovered in this research work was a rather high noise level in the output signal of the AGC circuit. The Spurious Free Dynamic Range (SFDR) was only 47 dB. When the VGA cell was replaced by the fixed gain amplifier, the SFDR changed to 63 dB, i.e. 16 dB better than in the AGC circuit. That suggested that the noise came from the VGA.

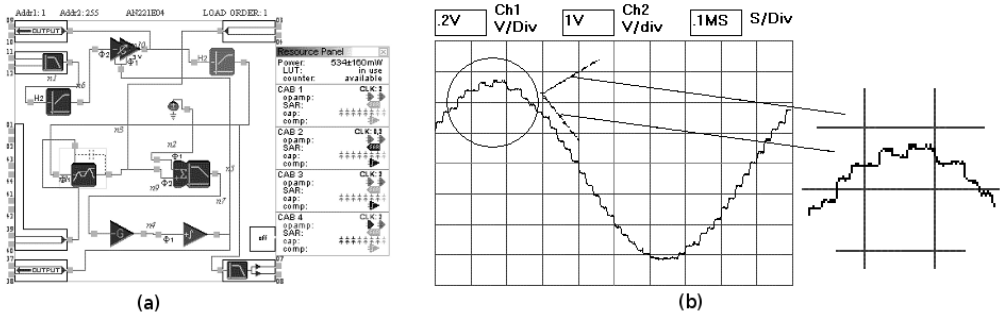

Fig. 3. AGC circuit. a) Block diagram; b) Output waveform

To understand the source of this noise the output waveform for sinusoidal input must be examined (Fig. 3b).

In the maximum region of the waveform (marked with a circle in Fig. 3b) small voltage steps can be observed. They result from the principle of VGA operation. The DC voltage of the integrator output is measured using an 8-bit SAR ADC, then the results are used as addresses for the LUT. The values contained in the LUT are used for setting the gain of the SC amplifier. A quantization error appears in the ADC, so successive results can differ by +/- 1, which results in step changes in the gain factor. The gain vs. control voltage characteristic is not continuous but is a stepwise function, so when the control voltage changes, we observe step changes in the output voltage. This fact leads to the conclusion that the observed noise is inevitable.

The described problem will appear in every circuit using the VGA cell based on the SC principle, not only the AGC circuit. The problem would not appear in the FPAAs built with the transconductance amplifiers or analog multipliers.

8. Dynamic reconfigurability

Anadigm dpASP devices can be reconfigured "on-the-fly" thanks to aforementioned split configuration memory. However, manufacturer's CAD software cannot make use of this capability. In order to test the reconfiguration ability of the FPAA, a program in VisualC# was written. The program is able to send reconfiguration data to the microcontroller which supervises the development kit. The FPAA then receives the data from the microcontroller. Transfer is indicated by pulling Config Flag (CFGFLG) pin low. The end of data transfer and configuration change is indicated by driving CFGFLG back high [19].

To examine the reconfiguration ability of the AN231 device, an oscillator circuit was chosen. Reconfiguration data was prepared in AnadigmDesigner2. A time graph of the reconfiguration process is presented in Fig. 4a. Channel 1 shows the output of the oscillator as a result of target frequency change from 40 to 80 kHz. Channel 2 shows a status signal taken from CFGFLG pin of the FPAA. It can be noticed that a change occurs at the same moment the CFGFLG pin is driven high. The frequency change is rapid and there is no step in amplitude or phase of the generated signal.

A similar circuit has been chosen for an examination of the AN221 device. The responses to frequency change and amplitude change were registered. Fig. 4b shows the output of the oscillator as a result of target frequency change from 20 kHz to 80 kHz. The change in the frequency is sharp, but the signal is continuous and its amplitude does not change.

Fig. 4c shows the output signal after a step change of the target amplitude. One can notice that the amplitude increases aperiodically to the new target value. The time constant of the response is about 150 μs.

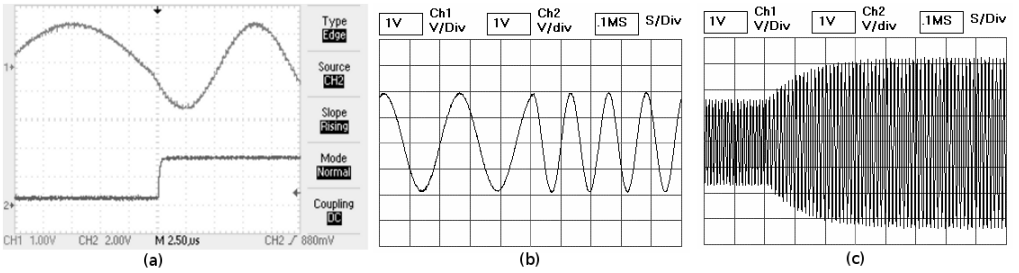

Fig. 4. Reconfiguration of examined devices. a) Sinewave oscillator frequency, AN231; b) Sinewave oscillator frequency, AN221; c) Sinewave oscillator amplitude, AN221

This confirms that the examined FPAAs are capable of "on-the-fly" reconfiguration without breaking the signal path.

9. Research on audio signal processing

One of the goals of this research was to determine if FPAAs can be utilized in audio processing applications. To verify that, some audio effect circuits described in [22] were designed and implemented using AN231E04 FPAA. Due to limitations of the development platform, the experiments were limited to standalone applications of the circuit. Exploring the capabilities of microprocessor-controlled FPAA applications is planned as a future work.

Every designed audio effect has been tested with an electronic keyboard, electric guitar and loudspeakers.

9.1 Tremolo effect

Tremolo is an effect of changing the amplitude of sound. It is implemented by using a simple amplitude modulator and a low-frequency oscillator (LFO). As the amplitude modulator, a multiplier CAM was used. The LFO is realized using a sinewave oscillator CAM clocked with 100 Hz frequency. The schematic of the effect is presented in Fig. 5a.

The lowest LFO output frequency obtained was 2 Hz. At lower frequencies the sinewave was distorted. An example of an 1 Hz waveform generated by LFO is shown in Fig. 5b.

In the Fig. 5c a time graph of a 750 Hz tone modulated by the designed tremolo effect circuit is shown.

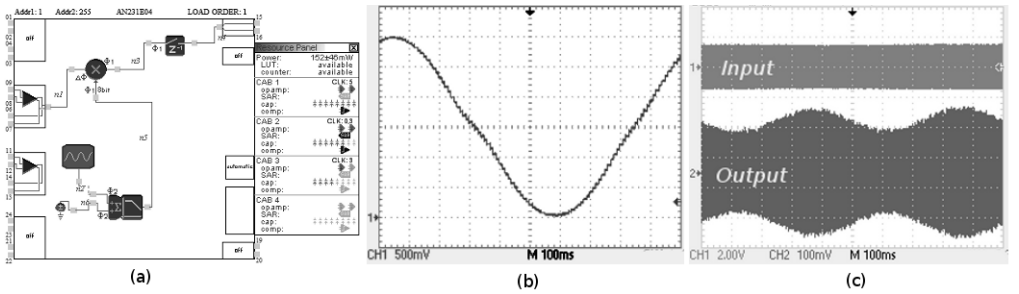

Fig. 5. Tremolo effect application. a) Schematic of the tremolo effect; b) Distorted 1 Hz sinewave generated by the LFO; c) Input and output signals of the tremolo

9.2 Infinite limiter (overdrive effect)

Limiting is a kind of dynamic range compression, limiting the gain of the circuit if the input signal is above a previously-set threshold. One of limiting variants is so-called “infinite limiting” or “clipping” [22]

A clipper circuit comprising a high-pass filter, a gain stage and a gain-limit stage has been realized. Its schematic is shown in the Fig. 6.

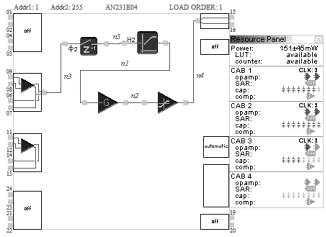

Fig. 6. A schematic of the infinite limiter

The HP filter is necessary to eliminate a DC component in the signal generated by an instrument. Without it, the DC component can overdrive the circuit.

There is no objective way of measuring the quality of the clipper effect. It can be rated only by hearing.

It is also possible to create other limiting or compressing circuits utilizing the AGC circuit presented in section 7.3.

9.3 De-esser

De-essing is a process of removing excess sibilant sounds from a recording or a live audio mix. There are several ways to achieve such an effect. Split-band de-essing was chosen and examined.

The designed circuit consisted of two filters (lowpass and highpass), a peak detector, a variable-gain amplifier and a summing block. The filters split the input signal into two subbands around the frequency of 2 kHz.

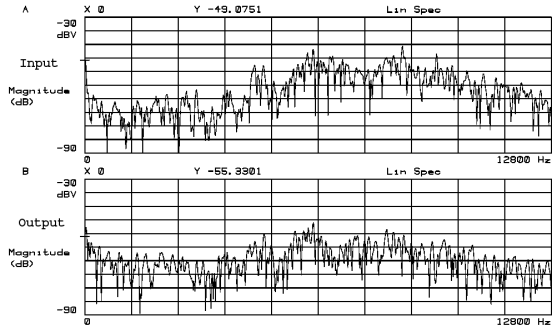

Fig. 7. Spectra of de-esser input (A) and output (B) signals

Fig. 7 presents spectra of the input and output signals of the de-esser. The spectra were measured when a previously-recorded sample of an „s” consonant was played by a PC connected to the de-esser’s input. It can be noticed in spectrum A that the „s” consonant has

most of its energy concentrated above 4 kHz. In spectrum B the part above 4 kHz is attenuated about 10 dB compared to spectrum A. This is considered to be a success and a proof that a simple de-esser circuit can be implemented using the examined FPAA.

9.4 Echo and delay effects

Neither echo nor delay effects can be implemented in a standalone FPAA due to a lack of an analog delay line capable of generating audible delays.

In order to create an audible effect, a delay of at least 10 milliseconds should be achieved. To create such a delay with a sampling frequency of 44100 Hz, a buffer of minimal length of 441 samples should be implemented. None of the available FPAA circuits is able to implement such a long buffer.

10. Conclusions

The presented research results presented show that AN221E04 and AN231E04 switched-capacitor FPAAs can be used for audio processing applications. It is possible to create some simple audio effects utilizing a stand-alone FPAA. The research also confirmed the proper "on-the-fly" reconfiguration capability of the FPAAs. However, the relatively high level of harmonic distortion limits its audio application to less-demanding devices.

Tested applications include a tremolo, a limiter and a de-esser circuit for the AN231 circuit and an Automatic Gain Control for the AN221 matrix. There is also a possibility of creating various types of audio filters up to 8th order. This is significantly simplified by the AnadigmFilter application included in the AnadigmDesigner2 package.

It is not possible, however, in a stand-alone FPAA application to change parameters of the circuit. To achieve the full functionality of audio effects it is required to adjust circuit parameters — for example the gain of the circuit or corner frequencies of the filters. Such functionality can be achieved in microprocessor-controlled applications, which are considered a field of future research. It is also interesting to determine the properties and scope of application of a bigger FPAA (for example 4 or 8 matrices connected together). FPAAs controlled by a PC with the AnadigmDesigner2 package can be widely used in educational applications. A single development board used as a students' laboratory research workstation can give them an opportunity to explore properties of switched-capacitor circuits as well as basic analog circuits like amplifiers, sample-and-hold circuits or filters.

Another application of the examined FPAAs is rapid prototyping. Dynamically programmable analog circuits give designers the opportunity to test designed solutions in significantly shorter time than when using conventional prototyping methods.

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